To achieve the necessary processing performance speeds, circuitry in IC’s is produced by applying multiple layers of metallization – six to eight layers is becoming increasingly common – onto the silicon substrate. During recent years, geometries have moved deep into the sub-micron realm and require a new level of accuracy in analytical and sample preparation tools.

This article discusses new ways in which optical alignment techniques may be used, in conjunction with improved polishing protocols, to improve the results available for the key sample preparation process of mechanical delayering of electronic circuitry.

<table>
<thead>
<tr>
<th>Calibration Measurement Device</th>
<th>Typical Accuracy of Measurement</th>
<th>Improvement due to optical alignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mechanical Indicator</td>
<td>1 to 2 microns</td>
<td>- -</td>
</tr>
<tr>
<td>ULTRACOLLIMATOR</td>
<td>0.1 microns</td>
<td>10x to 20x</td>
</tr>
<tr>
<td>Die Size ≤ 9mm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Die size 9mm to 18mm</td>
<td>0.2 microns</td>
<td>5x to 10x</td>
</tr>
</tbody>
</table>

Background - parallel polishing

To date the majority of mechanical deprocessing in the world has relied on a skilled analyst working with manual polishing tools, Cost-effective manual tools are available to be used with manual polishing stations. Manual techniques can yield good results over small die areas however results are not consistent from user to user.

Mechanical solutions for delayering that typically have been based on the sample die being mounted to a sample workholder, which is mechanically ‘calibrated’ to run relatively true to the rotating surface of the polisher below. As can be seen from Fig 2, the best digital indicators have a read-out accuracy of 1 micron, but a realistic accuracy of 1 –2 microns. Moreover older polishers are calibrated between the sample holder and the polishing surface (i.e. NOT the die directly). This introduces several unnecessary errors such as providing no ability to accommodate a difference in the wax thickness layer and the run-out of polishing plates, meaning that a high quality parallel polish across a significant portion of the die is almost impossible to achieve.

‘Fully Automated’ polishers have also been offered to the marketplace. These systems are extremely expensive, being affordable only for major fab-based labs, and have not addressed the basic need of enabling the analyst or technician to accurately and conveniently maintain planarity during the polishing operation, or to ‘end-point’ the process with suitable precision.

By use of optical alignment techniques, methods are now available that ensure sub-micron parallelism of the device under preparation can be maintained - even down to 0.1 microns for die sizes less than 9mm.
Background – polishing consumables

Key factors to success in parallel polishing are the correct selection and control of 1) Sample mounting & alignment, 2) Polishing Machine Variables and 3) Polishing Consumables.

1) Sample Mounting

Use of Quick Release fixtures allows for convenient transfer of the die between the polisher and the microscope. Sample holder design is discussed later in this article.

On older polishers any errors in mounting are compounded by the polishing technique. Fig 3 shows the way in which optical techniques can be used to calibrate (or ‘align’) direct to the die under test. This removes any mounting errors and produces a significant flatness and parallelism benefit.

![Fig 3 variation in wax thickness layer](image)

For the best results in parallel deprocessing it is usually best, where possible, for the passivation coating of the die under test to have been removed. This reduces polishing times and improves the planarity possible.

2) Polishing Machine Variables

The process settings for the polishing machine are critical to achieving optimum de-processing performance. Polishing repeatability is achieved through use of the moderate polishing speeds

3) Consumables

Edge rounding (roll-off) has long been the scourge of deprocessing on mechanical polishing machines. Through several previous generations of systems only passing regard has been made to improving the polishing pad dynamics to improve planarity across the die surface, from center to edge.

Pads and cloths do provide the means for producing highly specular (shiny) surfaces however, as shown in Fig 4, are generally too soft to be useful for optimized parallel polishing.

The use of hard surfaces based on polyurethane, is standard in production CMP processes provide a more rigid basis for reducing edge effects and are more resistant of the ‘trampoline’ effect seen with softer surfaces under pressure. Polyurethane-based materials also provide a good surface to be used in conjunction with colloidal silicas and aluminas, again the basic polishing used in CMP.

![Fig 4 earlier polishing cloth/parallel lapping method](image)

![Fig 5 improved hard surface/parallel lapping method](image)

As can be seen in Fig 5, the single die takes up only a small amount of the total wafer space. This means with that the improving total thickness variation (TTV) of wafers, the corresponding thickness variation over a single die will be negligible.

The key assumption of the technique when applied to deprocessing is that the backside of the die is parallel to the topside – this assumption is borne-out in practice. Even with a relatively large (TTV) across a wafer, the thickness variation across a single die is essentially negligible. With the TTV’s of modern wafers getting smaller, the dice are becoming ever more parallel. This also means that the backside surface is the best reference for alignment purposes. Moreover it remains so for the duration of during the polishing process.

![Fig. 5: This diagram shows the small percentage of the wafer surface taken up by a single die compared with the full wafer size. This ensures that the backside surface provides a parallel reference surface for topside delayering](image)
Optical Calibration—direct alignment to the die

The use of a direct line-of-sight between the backside of the die and the ULTRACOLLIMATOR. This is achieved by the design and implementation of equipment and sample holders that have a small hole to provide light access.

Autocollimation also requires that the backside of the die is polished – it is standard practice in ‘front end’ semiconductor processing, to allow for subsequent vacuum ‘pick and place’ during packaging. If the backside is not polished, for instance if the origin of the die is from wafer material (not from a package), the backside surface may be manually ‘buffed’ with a piece of diamond lapping film, to impart sufficient specularity, without varying the underlying parallelism profile.

Enabling layer by layer removal on smaller geometries

Autocollimation is an established optical industry technique for positioning lenses and key mechanical components. The ULTRA TEC ULTRACOLLIMATOR module incorporates the optical and control features required to adapt the technique for use in positioning a semiconductor die for accurate deprocessing. Fig 6 shows schematics of the ULTRACOLLIMATOR in both standard mode - used on MULTIPOL and other flat lapping machines, and the inverted mode – used on ASAP-1.

Key to both modes is the use of a reference flat and the ability to define the point of calibration – provided by a video-generated cross-hair - along with the relevant sample stage allowing for tilt adjustment, in order to align the device under test to the pre-defined reference point (Fig 7).

After alignment de-processing can be performed using standard process settings on the polisher. For a specific chemistry and die or sample size, the removal rate may be gauged using a time chart gained through empirical measurements.

Fig 7: Simple controls allow for rapid on-screen alignment of the die to the calibrated cross-hair
Selected Area Preparation: An accurate & convenient replacement for manual de-processing

Lab protocols for initial fault localization, such as liquid crystal, light or thermal emission, provide clues to localized area that contains the failure sites within the die. Topside physical removal of circuitry is then carried out to locate the failure.

Mechanical polishing allows for the failure to be precisely located. This operation requires not only a working knowledge of the circuitry layers within the device, but also a measure of skill and manual dexterity to be able to de-process the required area. Personnel possessing the skills require significant training and their loss to another department or organization can provide a big headache to the lab manager.

The use of semi-automatic machinery, such as ASAP-1 produces an immediate increase in alignment accuracy and process convenience. This leads to better operator-to-operator consistency and the potential to ‘de-skill’ the operation.

The utilization of a small diameter polishing tool, such as utilized by ASAP-1, yields significant benefits to the engineer…

◆ Polishing times are kept short due to the small area in contact with the polishing tool. Process convenience is optimized due to easy transfer and cleaning of the sample holder.

◆ The use of the instrument can be deskilled due to the increase in the consistency of polishing over manual techniques.

◆ Optical Alignment increases the size of the flat ‘sweet spot’, again making subsequent analysis of the device less challenging.

◆ The footprint of preparation equipment can be greatly reduced, since now a single multi-tasking unit can be used for both topside and backside preparation.

Fig 8: The image shows ASAP-1 with ULTRACOLLIMATOR optical upgrade. Also shown to the right of the sample mounting stage is a camera that allows for machine vision of the device under preparation.

Fig 9: The machine vision module on ASAP-1 ULTRACOLLIMATOR (6183.A) allows in-line monitoring of polishing progress.

Multi-layer chip sequentially deprocessed with ASAP-1

M6
M5
M4
M3
M2
M1
Poly

Note: die has 0.18micron technology; after Guerin/Obelin, ISTFA 2004
The Holy Grail: whole die delayering with true flat lapping techniques

The use of ‘on the lap’ polishing machines, such as MULTIPOL provides the means for much improved overall flatness of the sample being prepared.

This lapping concept is applied to the systems used for front-end CMP processing of full 200mm and 300mm wafers. Earlier ‘off the lap’ machines used in FA sample preparation do not achieve the level of flatness required.

‘On the lap’ polishing processes are slower than ‘off the lap’ processes due to the large amount of material in contact with the polishing surface. It is this degree of control that allows for a much higher accuracy and end-pointing.

As discussed earlier, the use of hard polyurethane-based polishing surfaces significantly reduces edge rounding. This, in conjunction with the greatly improved alignment available with the ULTRACOLLIMATOR, greatly increases the flat ‘sweet spot’ within the sample – often allowing for parallel delayering of the whole die simultaneously.

A large amount of research has taken place into the development of optimized colloidal silica slurries for specific chemistries (such as low-k’s). It may be found that to yield the best deprocessing results, it is worthwhile searching out the materials used for the front-end CMP.

The avoidance of cross-contamination and easy clean-up of the polishing machine should not be overlooked. On MULTIPOL this is achieved by a modular design which allows the slurry containment tray to be removed for cleaning, along with all the parts of the system that come into contact with polishing media.

The flat lapping polishing technique most suits the needs of the Reverse Engineer, who has the job of deprocessing a competitive Manufacturer’s die. This is the most demanding of all de-processing requirements, since a map generally must be made of the entire die at each of the metal layers – particularly where the design does not include repeating circuitry elements.

Yield Enhancement and failure analysis of wafer-level devices are also optimized by the use of a true flat lapping machine, such as MULTIPOL, where the resulting polishing flatness is much less sensitive to the size of the die under test, when compared to current ‘off the lap’ machines.
Quick Release Workholders: Rapid Transfer to & from optical and electron microscopes

The polishing techniques discussed here provide key performance improvements for deprocessing applications. The cornerstone instrument for analysis of the surfaces produces remains the optical microscope. As device sizes get smaller, however, the SEM is becoming invaluable.

The needs of the microscopist has driven the design of the sample holders and fixtures. Key design considerations and the resulting benefits are…

- Any sample holder must be conveniently mounted and transferred between the polishing machine and the microscope. This has been achieved by using a special ‘quick release’ cam-lock interface design.

- All sample holders should be low-relief allowing for positioning under all microscopes and objective set-ups.

- SEM’s generally require use of special stub holders, are best served by using sample holders that incorporate a suitable SEM-stub. This reduces time spent in on sample re-mounting.

- To allow for use with the optical alignments discussed here, sample holders must allow for direct line-of-sight between ULTRACOLLIMATOR and the wafer backside.

- Repeatable and easy-to-perform mounting techniques using Crystal Wax provide high strength and low-stress adhesion at relatively low temperatures.

To de-process exactly to the correct position in the layer of interest it is usually necessary to transfer between polisher and microscope many times during polishing. This means that the convenience and speed of transfer is of great importance and met by the “quick release” sample holders.

Cross-section holders for die and package-level components are also available and also benefit from the high degree of flatness possible with MULTIPOL.

![Fig 15: The ‘quick release’ SEM stub holder (6172.1) is optically-enabled and works for dice less than 10mm on a side. The holder allows for rapid transfer between polisher and SEM without the need to re-mount – an important time saver](image)

![Fig 16: A standard MULTIPOL ‘optical’ quick-release workholder (6170.1) provides line-of-sight for the ULTRACOLLIMATOR beam. The die is mounted over the center hole (left image). From the underside of the holder the backside of the die is visible through the center hole (right image). The workholder allows for convenient transfer between the polisher and the optical microscope](image)

![Fig 17: The ‘quick release’ sample holders are low relief, making them easy to view under any optical microscope. Shown here is the 6170.1 holder positioned under a 1.25X Macro objective (6601.1) on the ULTRA TEC Measuring Microscope (6680.1)](image)
Enabling Other Applications – Backside Preparation

Package-level backside preparation can also benefit from optical alignment techniques, particularly with an instrument using the inverted autocollimation mode, such as the ASAP-1.

The package is initially mounted in the inner inner pocket of a special flip-over sample holder.

After decapping the package through a standard selected area preparation (SAP) protocol (typically steps 1 and 2), to reveal the unthinned die backside, the package is cleaned and its holder is then ‘flipped’ so that the die’s backside is facing downwards in direct line of sight with the ULTRACOLLIMATOR camera.

After alignment, the inner pocket is flipped back to the starting position and the sample preparation process can proceed as normal. This method removes the need for operator estimation of the tilt correction, instead the autocollimator removes any guesswork. The improved sample alignment resulting form this allows for the production of thinner, flatter substrates on many package types and thus optimized imaging and more accurate backside analysis. The method particularly suits laser beam-based methods where the tolerance for a wedge in the remaining silicon is much less.

Conclusions

This article has detailed techniques that provide a major step forward in the parallel polishing of sub-wafer and die level devices. The systems that are used to implement these techniques have small footprint, are easy to use and affordable for all electronic analysis labs – Fab-based, fab-less and independent test labs can all benefit from optical alignment techniques.

The sample preparation needs of relevant lab functions- namely failure analysis, yield enhancement, and reverse engineering- all vary in their specific needs. Each of these fields benefits from one or more of the improved products and techniques discussed here.

The optical alignment and polishing machine design and consumables are all ‘future proof’. The availability of further improved alignment technologies and the ability of the analyst to springboard off the considerable expense and depth of research into front-end CMP applications means that there is a ready-made improvement path.

References & Further Reading

- International SEMATECH “Assembly analytical forum analytical tool roadmap white paper”, June 2004
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- G Gaut "The use of precision selective milling for failure analysis of flip-chip packages" ISTFA 2002

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Special Note: Many of the techniques and hardware items discussed in this article are PATENTED & PATENT PENDING.
### Selecting a De-processing Solution

<table>
<thead>
<tr>
<th></th>
<th>Failure Analysis</th>
<th>Yield Enhancement</th>
<th>Reverse Engineering</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process flexibility?</td>
<td>high</td>
<td>low</td>
<td>high</td>
</tr>
<tr>
<td></td>
<td>- many different types of packages, product returns</td>
<td>- usually wafer-level</td>
<td>- many different competitive analyses</td>
</tr>
<tr>
<td>Preparation Speed required?</td>
<td>high</td>
<td>medium to high</td>
<td>low</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- lower speed is acceptable trade-off for highest quality preparation results</td>
</tr>
<tr>
<td>Whole die delayer?</td>
<td>no</td>
<td>sometimes</td>
<td>yes</td>
</tr>
<tr>
<td></td>
<td>- unless the defect has not been located by ic or emission etc.</td>
<td></td>
<td>- especially with non-repeating circuitry designs</td>
</tr>
<tr>
<td>Equipment convenience required?</td>
<td>high</td>
<td>medium</td>
<td>low to medium</td>
</tr>
<tr>
<td></td>
<td>- should be deskilled to technician level</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sample Availability to user?</td>
<td>low</td>
<td>high</td>
<td>low</td>
</tr>
<tr>
<td></td>
<td>- often only one (failed) sample available</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Benefit from Optical Alignment?</td>
<td>yes</td>
<td>yes</td>
<td>yes</td>
</tr>
<tr>
<td>Benefit from multi-tasking equipment?</td>
<td>yes</td>
<td>yes</td>
<td>sometimes</td>
</tr>
<tr>
<td></td>
<td>- ASAP-1 also provides backside and decap capabilities</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Suggested preparation tool type</td>
<td>localized Area Polisher</td>
<td>localized area and/or flat polisher</td>
<td>flat polisher</td>
</tr>
<tr>
<td>Optimum polishing solution</td>
<td>ASAP-1</td>
<td>ASAP-1, MULTIPOL</td>
<td>MULTIPOL</td>
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#### Ordering Information

<table>
<thead>
<tr>
<th></th>
<th>ASAP-1</th>
<th>MULTIPOL</th>
</tr>
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<tbody>
<tr>
<td>System Order Code</td>
<td>6360.1</td>
<td>6108.5</td>
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<tr>
<td>ULTRACOLLIMATOR MODULE Order Code</td>
<td>6183.A</td>
<td>6183.M</td>
</tr>
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- also includes machine vision mode