Existing Technology

The State of the Art in Backside Sample Prep

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Backside analysis is more than just a way around the multi-metal nightmare for photoemission microscopy. Analysis from the substrate side is routine for a host of analytical methods such as LIVA, TIVA, XIVA, Laser Voltage Probe, and Thermal Schlieren imaging [3-7].

Backside preparation quality improved dramatically during the last year. No longer do the dies look like my glass shower door or are limited to 100 µm silicon thickness. New low speed milling and polishing methods make 30 µm substrates with a mirror finish routine. Even though the prep tools can now do a good job, there are still issues with sample prep. The main issue is whether the package interconnects interfere with the backside prep method, such as in type 2A BGA or CSP package types. There is also a trend away from "downset paddles" with leadless plastic chip carriers. The risks in these cases are severed wirebonds or circuit traces. Another issue with backside prep is fixturing. Great, I have this wonderfully prepped part that goes polished side face down in a conventional socket . . . now what? Currently, boards and sockets are butchered to accommodate this problem.

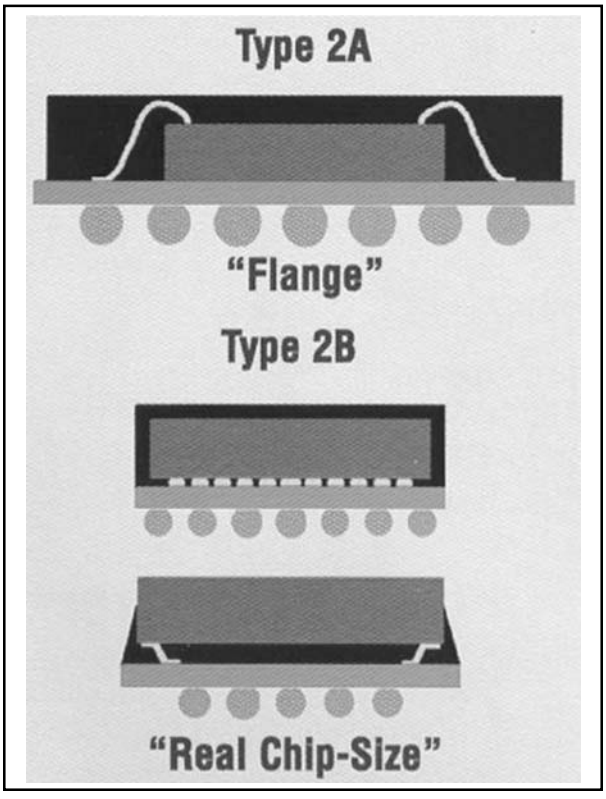

Fig. 1 *BGA package types*

There are two solutions. One is to rebond the part after backside sample preparation (unique failure) and the other is to select an appropriate package to wirebond a bare die of interest (multiple common failures)[6]. The second method is useful only for die-in-die form and not already packaged, such as for yield analysis. The first method assumes that the die is a unique failure already in the difficult package. These methods allow traditional fixturing, such as test heads and probe stations to be used in a normal test mode. No inverted boards cabled to a tester are needed since the die remains in its original package and is polished and rebonded to a new package carrier with the polished side facing upward. A simple pin reassignment corrects the reverse wire sequence after wire-to-wire bonding or wire-to-frame bonding in the new package frame. The resulting orientation eliminates many backside microscopy problems since the resulting package orientation is now frontside. The low profile, wedge bonds allow short working distance objectives, such as immersion lenses, to be used across the die surface. Test equipment can be used with analytical tools such as the emission microscope or focused ion beam due to the upright orientation of the polished backside silicon.

The BGA and Chip Scale Package Problem

Type 2A BGA packages cannot be prepared for backside analysis due to the location of the PCB and because balls require wire-to-wire bonding. Figure 1 shows three package types. The type 2B and "real chip size" packages can be prepared by mounting the ball side to the polishing fixture and polishing the die directly. Figure 2 shows a more challenging

Portions of this article are extracted from "BBGA and Advanced Package Wire to Wire Bonding for Backside Emission Microscopy," *Proc. Of ISTFA 1999*,[1] as well as Patent #6245586.[2]

package. This package is a stacked design. Electrical determination of the failing chip dictates whether the SRAM or the Flash die is the polish target for wire-to-wire bonding. Figure 3 shows a 3D multi-chip chip scale package. If the lower die is the analysis target, then the package is prepared in the same manner as a type 2B. If the upper die is the target, then the part is prepared the same as type 2A.

Determining Die Thickness During Sample Preparation

The thickness of the remaining silicon can be determined by focal depth measurements on a microscope equipped with near infrared illumination where

$$\Delta F * n \cong t \qquad \text{(Eq 1)}$$

and

ΔF = Difference in focus from polished surface to circuit

n = Index of refraction of the silicon

t = thickness

The focal distance from the polished surface to the metallization multiplied by 3.434 equals the thickness of the remaining silicon at a wavelength of 1064 nm. This is the basis for determining tilt as well as thickness of the remaining silicon. The Mitutoyo focus block on the microscope is graduated in microns. Error calibration is done with the chosen microscope objective (100X NIR) and a sample of known thickness. The index of refraction combined with the error factor is calculated for this focus mechanism by dividing the known thickness of a wafer by the focus distance from surface to circuit (249 µm / 68 µm = 3.66). I used n=3.66 for silicon for this focal measurement method. The error in precision is compounded by the index of refraction multiplier, making precise focal point measurements tedious.

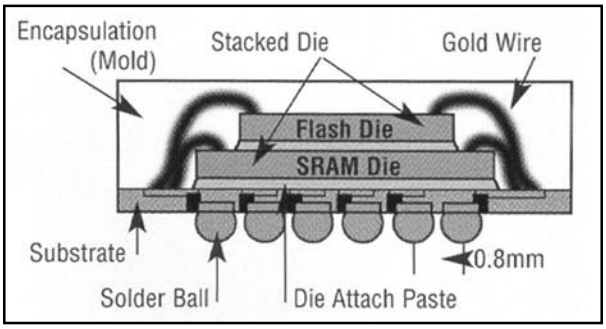

Fig. 2 *Chip scale package*

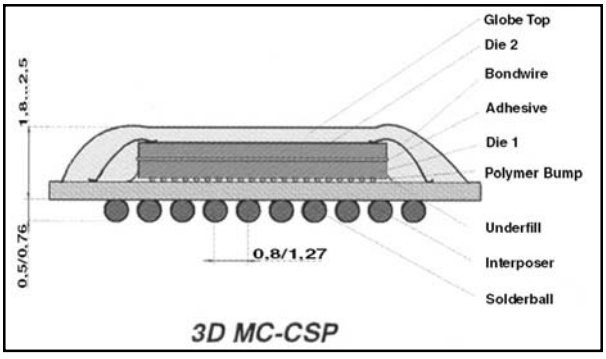

Fig. 3 *Schematic of CSP from MPD showing stacked chips*

Preparation of PQFP Type Packages for Wire to Wire Bonding

A 100-pin PQFP cache RAM illustrates the wire-to-wire preparation process. The integrated circuit that is prepared for backside imaging is already packaged in a typical plastic epoxy package. If the package is of the open cavity (ceramic) or soft cavity type (such as with a diecoat), then the cavity must be filled with a rigid material, such as room temperature cure epoxy, prior to polishing or lapping the package material. Do not use a high temp epoxy! The stress of thermal contraction of the epoxy against the thinned die will distort and destroy it. In this case, a standard molding compound is the encapsulant without die coat. The die and package are thinned to the target thickness combining 600 to 1200 grit sandpaper finishing with a colloidal silica polish. The leadframe is eliminated during this thinning step to expose the embedded bond wires. Focal depth measurements determine the amount of remaining silicon.

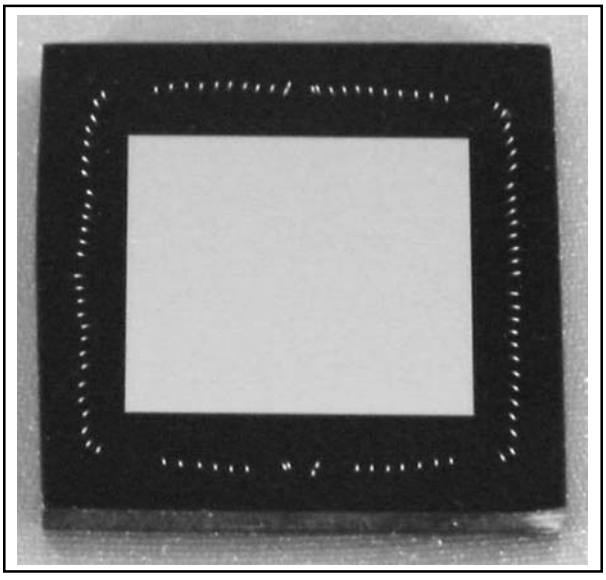

Fig. 4 *Original package after preparation*

Since the silicon die is still embedded in the original package, the package acts as a carrier for the die. Depending on the nature of the package and die, the leadframe will be intact, partially polished, or completely polished away. If the leadframe is intact, a probecard or socket can make electrical contact to the die through the remaining leadframe or with wirebonding. If the leadframe is gone, the wires that are bonded to the die will be visible, embedded in the plastic at the polished surface. Mechanical probes contact the embedded wires; however, the number of pins is usually a limiting factor to probes.

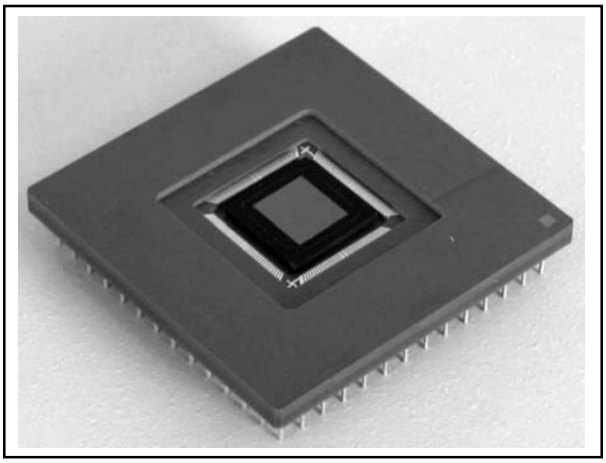

Fig. 5 *The sample is die attached with room temp. epoxy to a 132 lead ceramic pin grid array and wire bonded*

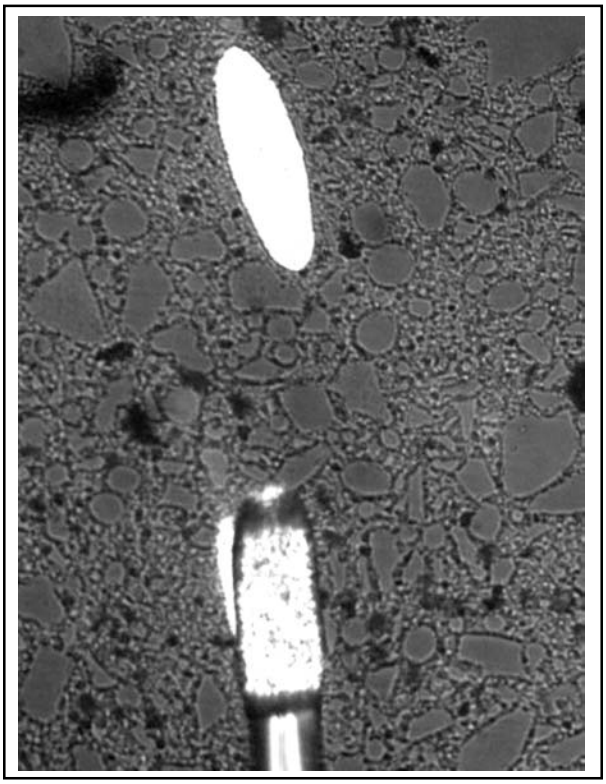

Fig. 6 *View of the wedge bond associated with one of two identical power pins. The other was left intentionally unbonded for illustration purposes.*

Wafers can also be prepared for backside by dicing the wafer and wirebonding the die conventionally into an open leadframe or package. If an open leadframe is used, it can be encapsulated with room temp. epoxy prior to backside preparation. The chip is sized by sanding the excess plastic material from the edges and thinning the top if necessary (to fit in the new die cavity), being careful not to disturb the wire loops embedded in the plastic package. The polished chip embedded in the remaining epoxy can now be treated as an integrated circuit die. The embedded wires at the surface serve as bond pads and the polished backside is now considered the top surface (Fig. 4). The resulting part is attached to a new package and wire bonded to create electrical connections between the die and new leadframe. The polished interface must be clean for the bonding process to work. Maximum power at room temperature allows acceptable aluminum wedge bonds to the gold wire interface. Figures 5 and 6 are optical photos of a section of the finished product. The new pinout is implemented on the loadboard or a socket wiring adapter is used with the existing loadboard.

Preparation of a Type 2A 312 BGA Package for Wire-to-Wire Bonding

Type 2A BGA packages follow the same preparation

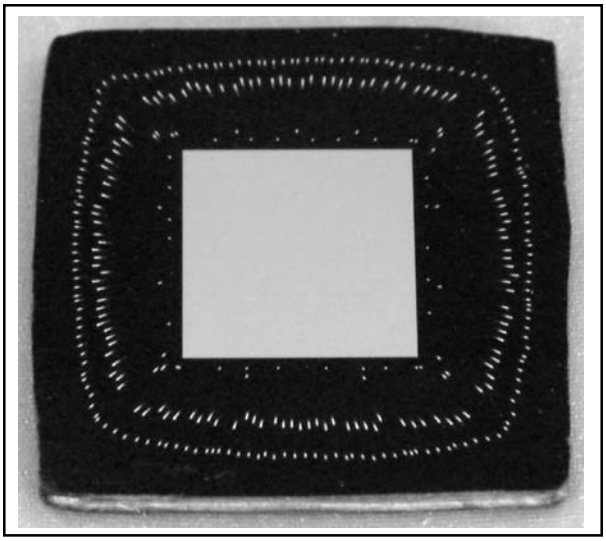

Fig. 7 *Polished BGA die in the original package ready for die attach and wire-to-wire bonding in a new package*

methods with a target of 20 µm thick. The balls and board are sacrificed. Once the target thickness is reached, the part is ready for wire-to-wire bonding into a new package. In this case, the outside dimensions in Fig. 7 are 15 mm × 15 mm.

Achieving a Thin, Flat, and Defect Free Surface Using a Diamond Mill

The pocket mill method for backside prep began with high speed diamond mills and is evolving to gentle low speed mills, driven by the need for surface quality and thinner substrates. The low speed diamond mill process can perform wire-to-wire bonding just as the planar lapping method. Die bow is frequently seen immediately after the copper paddle is removed. Surprisingly, this effect can typically be ignored as the die and package will "relax" by the time the target thickness is achieved. If an encapsulant has an extreme CTE (coefficient of thermal expansion), the die will shatter no matter what you do. This has only been seen to date with high temp. cure epoxies used to fill the cavity after a frontside analysis.

Anti-Reflective Coatings (ARC)

ARC coatings are quite beneficial for backside imaging and analysis. About 60% of the light is scattered when using coaxial illumination without an ARC coat (Fig. 8) and 30% of emission microscopy sensitivity is lost without it. Image quality rivals frontside when ARC is used if the substrate is not heavily doped and a smooth surface is achieved.

A good reference paper for traditional ARC is by Brennan Davis[8]. Today, ARC can be vacuum deposited or spun on. A new method of ARC deposition allows wire-to-wire bonded parts as well as traditional parts to be coated using a spin-on coating process at ambient temperature. The coating is easily removed and reapplied as needed using a machine called the ARC-lite from Ultra Tec (Santa Ana, Calif.). With thin silicon and ARC coatings, high magnification views of the circuitry is possible, rivaling frontside images as shown in Fig. 8.

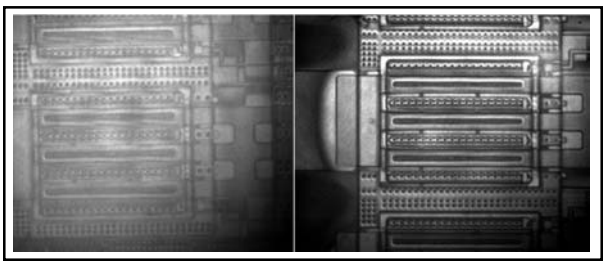

Fig. 8 *The finished product with ARC coating on the right and none on the left. (100× NIR objective)*

Conclusion

New preparation methods were discussed for achieving clean backside surfaces as well as ARC. Wire-to-wire bonding preparation was done on either Ultra Tec or Allied High Tech equipment with flat lapping capabilities. An Ultra Tec ASAP-1 was used for backside diamond mill and polish methods in both traditional and wire-to-wire bond cases. High-speed mills are not recommended in order to maintain the bond interface integrity as well as sample finish requirements. Backside analysis evolved to allow an integrated circuit that is already encapsulated in a plastic package as well as to allow individual dies to be polished from the backside and electrically connected to a new package. The resulting orientation eliminates many of the problems of backside microscopy since the resulting package orientation is now frontside. Test equipment can be used with analytical tools, such as the emission microscope or focused ion beam, due to the upright orientation of the polished backside silicon. It is obvious that this method can intercept the electrical connection of a variety of package types such as Ball Grid Array, Pin Grid Array, PLCC (Plastic Leaded Chip Carrier), QFP (Quad Flat Pack), DIP (Dual Inline Pack), CSP (Chip Scale Package), and SOIC (Small Outline Integrated Circuit). Flip chip technologies can be polished using the methods outlined above. Various surface probe and imaging techniques are now quite viable from the backside due to the flat profile of the new sample preparation.

Acknowledgments

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References

1. J. Colvin: "BGA and Advanced Package Wire-to-Wire Bonding for Backside Emission Microscopy," *Proc. of ISTFA,* ASM International, 1999, pp. 365-75.

2. Patent # 6245586 (Colvin): "Wire-to-Wire Bonding System and Method."

3. E.I. Cole Jr., J.M. Soden, J.L. Rife, D.L. Barton, and C.L. Henderson: "Novel Failure Analysis Techniques Using Photon Probing in a Scanning Optical Microscope," *Proc. of IRPS,* IEEE, Piscataway, N.J., 1994, pp. 388-98.

4. E.I. Cole Jr., P. Tangyunyong, and D.L. Barton: "Backside Localization of Open and Shorted IC Interconnections," *Proc. of IRPS*, IEEE, Piscataway, N.J., 1998, pp. 129-36.
5. R. A. Falk: "Advanced LIVA/TIVA Techniques," *Proc. of ISTFA,* ASM International, 2001, pp. 59-65.
6. S. Kolachina, K.S. Wills, T. Nagel, A. Mehta, R. Carawan, O. Diaz de Leon, J. Grund, C.P. Todd, K. Ramanujachar, S. Nagarathnam, C. Charpentier, D. Gobled, W. Subido: "Optical Waveform Probing – Strategies for Non-Flipchip Devices and Other Applications,"*Proc. of ISTA*, ASM International, 2001, pp. 51-8.
7. R.A. Falk: "Application of Near IR, Phase Contrast to Backside Failure Isolation and Analysis," *Proc. of ISTFA,* ASM International, 2000, pp. 567-73..
8. B.V. Davis: "Antireflection Coatings for Semiconductor Failure Analysis," *Proc. of ISTFA,* ASM International, 2000, pp. 155-60.

Related Reference

S. Liebert: "Failure Analysis from the Back Side of a Die," *Proc. of ISTFA,* ASM International, 2001, p 177-85.

About the Author

Jim Colvin has published at both ISTFA and IRPS on Atomic Force Microscopy and EOS/ESD. He gave the "Atomic Force and Scanning Probe Microscopy Seminar" at ISTFA from 1993 to 1995. He is past secretary and workshop chair on the Steering Committee of the EOS/ESD symposium and chair of the SPM Committee for ISTFA 2002. He received the Best Paper award from the EOS/ESD Symposium in 1993 and the Outstanding Paper Award from ISTFA in 1995. Colvin was also chair of the IEEE Reliability Society for three years. He has six patents plus three pending.